RAMAIAH
Institute of Technology

CURRICULUM

for the Academic Year 2021 – 2022

(Batch of 2021 – 2023)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

M. Tech (VLSI DESIGN AND EMBEDDED SYSTEMS)

I – IV Semester M. Tech

RAMAIAH INSTITUTE OF TECHNOLOGY
(Autonomous Institute, Affiliated to VTU)
Bangalore – 560054.

About the Institute

Dr. M. S. Ramaiah a philanthropist, founded 'Gokula Education Foundation' in 1962 with an objective of serving the society. M S Ramaiah Institute of Technology (MSRIT) was established under the aegis of this foundation in the same year, creating a landmark in technical education in India. MSRIT offers 17 UG programs and 15 PG programs. All these programs are approved by AICTE. All eligible UG and PG programs are accredited by National Board of Accreditation (NBA). The institute is accredited with **'A^{+}' grade by NAAC in March 2021** for 5 years. University Grants Commission (UGC) & Visvesvaraya Technological University (VTU) have conferred Autonomous Status to MSRIT for both UG and PG Programs since 2007. The institute is a participant to the Technical Education Quality Improvement Program (TEQIP), an initiative of the Government of India. The institute has 380 competent faculty out of which 60% are doctorates. Some of the distinguished features of MSRIT are: State of the art laboratories, individual computing facility for all faculty members, all research departments active with sponsored funded projects and more than 300 scholars pursuing Ph.D. To promote research culture, the institute has established Centre of Excellence for Imaging Technologies, Centre for Advanced Materials Technology, Centre for Antennas and Radio Frequency systems (CARFS), Center for Cyber Physical Systems & Schneider Centre of Excellence. **M S Ramaiah Institute of Technology has obtained "Scimago Institutions Rankings" All India Rank 65 & world ranking 578 for the year 2020.**

The Entrepreneurship Development Cell (EDC) and Section 8 company "Ramaiah Evolute" have been set up on campus to incubate startups. **M S Ramaiah Institute of Technology secured All India Rank 8th for the year 2020 for Atal Ranking of Institutions on Innovation Achievements (ARIIA), by MoE, Govt. of India.** MSRIT has a strong Placement and Training department with a committed team, a good Mentoring/Proctorial system, a fully equipped Sports department, large air-conditioned library with good collection of book volumes and subscription to International and National Journals. The Digital Library subscribes to online e-journals from Elsevier Science Direct, IEEE, Taylor & Francis, Springer Link, etc. MSRIT is a member of DELNET, CMTI and VTU E-Library Consortium. MSRIT has a modern auditorium and several hi-tech conference halls with video conferencing facilities. The institute has excellent hostel facilities for boys and girls. MSRIT Alumni have distinguished themselves by occupying high positions in India and abroad and are in touch with the institute through an active Alumni Association.

As per the National Institutional Ranking Framework (NIRF), MoE, Government of India, M S Ramaiah Institute of Technology has achieved 65th rank among 1143 top Engineering institutions of India for the year 2021 and is 1st amongst the Engineering colleges affiliated to VTU, Karnataka.

About the Department

The Department of Electronics and Communication was started in 1975 and has grown over the years in terms of stature and infrastructure. The department has well equipped simulation and electronic laboratories and is recognized as a research center under VTU. The department currently offers a B. E. program with an intake of 120, and two M. Tech programs, one in Digital Electronics and Communication, and one in VLSI Design and Embedded Systems, with intakes of 30 and 18 respectively. The department has a Center of Excellence in Food Technologies sponsored by VGST, Government of Karnataka. The department is equipped with numerous UG and PG labs, along with R & D facilities. Past and current research sponsoring agencies include DST, VTU, VGST, ISRO and AICTE with funding amount worth Rs. 1 crore. The department has modern research ambitions to develop innovative solutions and products and to pursue various research activities focused towards national development in various advanced fields such as Signal Processing, Embedded Systems, Cognitive Sensors and RF Technology, Software Development and Mobile Technology.

Vision of the Institute

To be an Institution of International Eminence, renowned for imparting quality technical education, cutting edge research and innovation to meet global socio-economic needs

Mission of the Institute

RIT shall meet the global socio-economic needs through

- *Imparting quality technical education by nurturing a conducive learning environment through continuous improvement and customization*
- *Establishing research clusters in emerging areas in collaboration with globally reputed organizations*
- *Establishing innovative skills development, techno-entrepreneurial activities and consultancy for socio-economic needs*

Quality Policy

We at M. S. Ramaiah Institute of Technology strive to deliver comprehensive, continually enhanced, global quality technical and management education through an established Quality Management System complemented by the synergistic interaction of the stake holders concerned

Vision of the Department

To evolve into a department of national and international repute for excellence in education and cutting-edge research in the domain of Electronics and Communication Engineering

Mission of the Department

The department will continuously strive to

1. *Provide a world-class learning environment that caters to local and global technological and social requirements*
2. *Initiate research collaborations with academia and industries to perform cutting edge research leading to socio-technological innovations*
3. *Develop skills for pursuing innovation and entrepreneurial ventures for graduating engineers*

Program Educational Objectives (PEOs)

PEO1: *Be successful practicing professionals or pursue doctoral studies in areas related to the program, contributing significantly to research and development activities*

PEO2: *Engage in professional development in their chosen area by adapting to new technology and career challenges*

PEO3: *Demonstrate professional, ethical, and social responsibilities of the engineering profession*

Program Outcomes (POs)

PO1: ***Development of Solutions:*** *An ability to independently carry out research/investigation and development work to solve practical problems*

PO2: ***Technical Presentation Skills:*** *An ability to write and present a substantial technical report/document*

PO3: ***Analyze Complex Systems:*** *A practical ability and theoretical knowledge to design and analyze VLSI and embedded systems*

PO4: ***Develop Novel Designs:*** *An ability to apply their in-depth knowledge in VLSI and embedded systems domain to evaluate, analyze and synthesize existing and novel designs*

PO5: ***Team Work and Project Management:*** *An ability to effectively participate as a team member and develop project management skills necessary for a professional environment*

CURRICULUM CREDITS DISTRIBUTION

Semester	Professional Courses – Core (Theory and Lab) (PC-C)	Professional Courses – Electives (PC-E)	Technical Seminar (TS)	Project Work/Internship (PW/IN)	Credits in a semester
First	10	12	2	-	**24**
Second	10	12	2	-	**24**
Third	4	4	-	10	**18**
Fourth	-	-	-	22	**22**
Total	**24**	**28**	**4**	**32**	**88**

SCHEME OF TEACHING

M. Tech (VLSI DESIGN AND EMBEDDED SYSTEMS)

(Batch 2021 – 2023)

I SEMESTER

SI. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE11	Advanced Engineering Mathematics	PS-C	3	1	0	4	5
2.	MVE12	VLSI Circuits and Systems	PS-C	4	0	0	4	4
3.	MVEExx	Elective 1	PS-E	4	0	0	4	4
4.	MVEExx	Elective 2	PS-E	4	0	0	4	4
5.	MVEExx	Elective 3	PS-E	4	0	0	4	4
6.	MVEL13	Digital System Design Laboratory	PS-C	0	0	1	1	2
7.	MVEL14	Advanced Embedded Systems Laboratory	PS-C	0	0	1	1	2
8.	MVE15	Technical Seminar I	TS	0	0	2	2	4
Total				**19**	**1**	**4**	**24**	**29**

II SEMESTER

SI. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE21	Analog and Mixed Signal IC Design	PS-C	4	0	0	4	4
2.	MVE22	Advanced Microcontrollers	PS-C	4	0	0	4	4
3.	MVEExx	Elective 4	PS-E	4	0	0	4	4
4.	MVEExx	Elective 5	PS-E	4	0	0	4	4
5.	MVEExx	Elective 6	PS-E	3	1	0	4	5
6.	MVEL23	Analog and Mixed Signal IC Design Laboratory	PS-C	0	0	1	1	2
7.	MVEL24	Advanced Microcontroller Laboratory	PS-C	0	0	1	1	2
8.	MVE25	Technical Seminar II	TS	0	0	2	2	4
Total				**19**	**1**	**4**	**24**	**29**

III SEMESTER

SI. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE31	Low Power VLSI Design	PC-C	4	0	0	4	4
2.	MVEExx	Elective 7	PC-E	4	0	0	4	4
3.	MVE32	Internship/Industrial Training	IN	0	0	4	4	8
4.	MVE33	Project Work – I	PW	0	0	6	6	12
Total				**8**	**0**	**10**	**18**	**28**

IVSEMESTER

SI. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE41	Project Work – II	PW	0	0	22	22	44
Total				**0**	**0**	**22**	**22**	**44**

LIST OF ELECTIVES

SI. No.	Course Code	Course Title	Credits			
			L	T	P	Total
1.	MVEE01	Advanced Embedded Systems	4	0	0	4
2.	MVEE02	Digital System Design using HDL	4	0	0	4
3.	MVEE03	Digital VLSI Testing	4	0	0	4
4.	MVEE04	Advanced Digital Logic Verification	4	0	0	4
5.	MVEE05	MEMS and Nanoelectronics	4	0	0	4
6.	MVEE06	Machine Learning & Deep Learning	4	0	0	4
7.	MVEE07	Internet of Things (IoT)	4	0	0	4
8.	MVEE08	Physics of Semiconductor Devices	4	0	0	4
9.	MVEE09	Synthesis and Optimization of Digital Circuits	4	0	0	4
10.	MVEE10	ASIC Design	4	0	0	4
11.	MVEE11	System on Chip Design	4	0	0	4
12.	MVEE12	Physical VLSI Design	4	0	0	4
13.	MVEE13	Advanced Computer Architecture	4	0	0	4
14.	MVEE14	VLSI Signal Processing	4	0	0	4
15.	MVEE15	Memory Technologies	4	0	0	4
16.	MVEE16	Communication Busses and Interfaces	4	0	0	4

ADVANCED ENGINEERING MATHEMATICS

Course Code: MVE11 **Credits: 3:1:0**

Prerequisites: Engineering Mathematics **Contact Hours: 70**

Course Coordinator: M. Girinath Reddy

UNIT – I

Linear Algebra I: Geometry of linear equations, Solution sets of linear systems, Gaussian elimination method, Gauss Seidel method, Matrix notation, inverses, Partitioned matrices, Matrix factorization and determinants

UNIT – II

Linear Algebra II: Linear transformations, Composition of matrix transformations, Rotation about the origin, Dilation, Contraction and Reflection, Vector spaces and subspaces, linear independence, rank, basis and dimension, linear transformation, change of basis

UNIT – III

Graph Theory: Introduction, Isomorphism, Connected Graphs, Disconnected Graphs, Trees, Cut-sets, Vectors spaces of Graphs, Electrical network analysis by graph theory

UNIT – IV

Linear Differential Equations: Definitions, complete solutions, rules for finding the complementary function, inverse operator, rules for finding the particular integral, Cauchy's and Legendre's linear equations, linear dependence of solutions, simultaneous linear equations with constant coefficients

UNIT – V

Partial Differential Equations: Introduction, formation of partial differential equations, solutions of partial differential equations, homogeneous linear equations with constant coefficients, working procedure to solve homogeneous linear equations, rules for finding complementary function, non-homogeneous linear equation

References:

1. Gareth Williams, "Linear Algebra with Applications", 6th Edition, Jones and Barlett Publishers, 2011
2. David C Lay, "Linear Algebra and its Applications", 3rd Edition, Pearson Education, 2013

3. Narsingh Deo, “Graph Theory with Applications to Engineering and computer Science”, PHI Learning, 2011
4. B.S. Grewal, “Higher Engineering Mathematics”, 44th Edition, Khanna Publication, 2018

Course Outcomes (COs):

1. Solve linear equations using Gauss elimination and Gauss Seidel methods (POs: 1, 3)
2. Verify if the given set forms a basis of a vector space and change the bases in the vector space (POs: 1, 3)
3. Use graph theoretic idea for electrical network analysis (POs: 1, 3)
4. Use analytical methods to solve higher order ordinary differential equations and simultaneous differential equations a raising in many practical applications (POs: 1, 3)
5. Learnt to form and solve PDE’s for homogeneous and non- homogeneous linear equations (POs: 1, 3)

VLSI CIRCUITS AND SYSTEMS

Course Code: MVE12 **Credits: 4:0:0**

Pre requisites: Digital Design **Contact Hours: 56**

Course Coordinator: V Anandi

UNIT – I

MOS Transistor Theory: n MOS/p MOS transistor, Threshold voltage equation, Body effect, MOS device design equation, Sub-threshold region, Channel length modulation, Mobility variation, Tunneling, Punch through, Hot electron effect MOS models, Small signal AC characteristics, CMOS inverter, βn/βp ratio, Noise margin, Static load MOS inverters, Transmission gate, Tristate inverter

UNIT – II

Circuit Characterization and Performance Estimation: Delay Estimation – transient response, RC delay model, Elmore delay model, Linear delay model, Sizing with the method of logical effort

Combinational and Sequential Circuit Design: Static CMOS, CMOS circuit design families: CVSL, Pseudo nMOS, Pass transistor circuits, Sequential circuits: circuit design of latches and flip-flops

UNIT – III

Data Path Sub System Design: Introduction, Addition – Carry lookahead, Carry Select, Tree Adders – Brent Kung, Kogge Stone, Sklansky, Subtraction, Multiplication: Carry-Save format, Booth Algorithm, Comparators, Counters, Boolean logical operations, Coding, Shifters

UNIT – IV

Dynamic CMOS and Clocking: Introduction, Advantages of CMOS over NMOS, CMOS/SOS technology, CMOS/bulk technology, Latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking – clock generation, clock distribution, clocked storage elements

UNIT – V

Timing Issues in Digital Circuits: Timing classification of digital systems, Synchronous design – Timing basics, Skew and Jitter, Latch based techniques, Self-timed circuits, Synchronization and arbiters

References:

1. Neil H E Weste, David Harris, "CMOS VLSI Design: A System Perspective", 4th Edition, Pearson Education, 2014.
2. Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated circuits: A design perspective" 2nd Edition, Pearson Education,2016.
3. Wayne Wolf, "Modern VLSI Design: System on Silicon", 3rd Edition, PHI, 2008.
4. Douglas A Pucknell, Kamran Eshraghian, "Basic VLSI Design", 3rd Edition, PHI,2009.
5. Sung Mo Kang, Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", 3rd Edition, Tata McGrawHill, 2003.

Course Outcomes (COs):

1. Recall basics of CMOS digital integrated circuits. (POs:1, 3, 4)
2. Employ different performance metrics to predict the performance of VLSI circuits. (POs:1, 3, 4)
3. Apply digital design concepts to demonstrate different data path functions. (POs: 1, 3, 4)
4. Design and analyze dynamic CMOS circuits. (POs: 1, 3, 4)
5. Analyze variations in clock signals, and design circuits to reduce effects of large clock distribution networks. (POs: 1, 3, 4)

DIGITAL SYSTEM DESIGN LABORATORY

Course Code: MVEL13 **Credits: 0:0:1**

Prerequisites: Digital Electronics **Contact Hours: 28**

Course Coordinator: S. L. Gangadharaiah

LIST OF EXPERIMENTS

Using Verilog code design, simulate and synthesize the following with a suitable FPGA.

1. 8 to 3 programmable priority encoder
2. Full Adder using structural modeling
3. Flip Flops(D,SR,T,JK)
4. 4-bit arbitrary counter,4-bit binary up/down/up-down counter with synchronous reset, 4-bit Johnson counter, BCD counter
5. Sequential block to detect a sequence (say 11101) using appropriate FSM
6. 8-bit ripple carry adder and carry skip adder
7. 8-bit carry select adder
8. Stepper motor and DC motor interface
9. DAC interface

Using System Verilog code, simulate the following

10. Full subtractor using structural modeling
11. Flip Flops(D,SR,T,JK)
12. 4-bit synchronous/asynchronous counters, synchronous arbitrary counters

References:

1. Peter J. Ashenden, “Digital Design: An Embedded Systems Approach using Verilog”, Elsevier, 2010.
2. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, 2nd Edition, Pearson Education, 2010.
3. Stuart Sutherland, “RTL Modeling with System Verilog for Simulation and Synthesis: using System Verilog for ASIC and FPGA Design”, 1st Edition, Create Space Independent Publishing Platform, 2017.

Course Outcomes (COs):

1. Design and model complex combinational circuits using HDL at behavioral, structural and RTL levels. (POs: 1, 3, 4, 5)
2. Enumerate complex sequential circuits using HDL at behavioral, structural and RTL levels. (POs: 1, 3, 4, 5)
3. Develop test benches to simulate combinational and sequential circuits. (POs: 1, 3, 4, 5)
4. Illustrate how the language infers hardware and helps to simulate and synthesize the digital system. (POs: 1, 3, 4, 5)
5. Implement and analyze the digital systems using FPGAs with respect to speed and area. (POs: 1, 3, 4, 5)

ADVANCED EMBEDDED SYSTEMS LABORATORY

Course Code: MVEL14 **Credits: 0:0:1**

Prerequisites: Embedded Systems **Contact Hours: 28**

Course Coordinator: K. V. Suma

LIST OF EXPERIMENTS

Part A – PCB Designing

1. Generation of schematic – Opamp Circuit
2. Generation of layout – Opamp Circuit
3. Circuit selection
4. Bill of materials and Netlist
5. Layouts and routing of the circuit
6. Gerber file generation and online viewer

Part B – Unified Modeling Language (UML)

7. Model the static aspects of the system using Use Case diagram in UML
8. Model the static aspects of the systemusing
    a. Basic Class diagram and generate code in UML
    b. Optimize Class diagram and generate code in UML
9. Model the elevator system using Sequence diagram in UML

Part C – RTOS programs

10. Program in C to create a process using fork() function call (forkdemo.c) and to simulate in Linux platform
11. Program in C to generate a signal when a delete key is pressed (signal) and to simulate in Linux platform

Reference:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M4", 3rd Edition, Newnes, (Elsevier), 2014.

Course Outcomes (COs):

1. Generate the schematic, netlist, bill of materials and layout for PCB of a given circuit. (POs: 3, 5)
2. Derive Gerber files for actual PCB fabrication. (POs: 4, 5)
3. Illustrate UML static diagrams for a given embedded application. (POs: 1, 3, 4, 5)
4. Develop UML dynamic diagrams for a given embedded application. (POs: 1, 3, 4, 5)
5. Implement the basic concepts of RTOS such as threads and processes. (POs: 4, 5)

TECHNICAL SEMINAR – I

Course Code: MVE15 **Credits: 0:0:2**

Prerequisites: Nil **Contact Hours: 56**

LIST OF ACTIVITIES

1. Seminar: Research Methods
2. Seminar: Technical Report Writing
3. Source/Ideas for a Research Problem
4. Choosing Research Papers
5. Reading Research Papers
6. Summarizing Research Papers: Written
7. Presenting Research: Oral
8. **REVIEW – I**
9. Critiquing: Oral & Written
10. Detailed analysis of Block Diagrams: Written
11. Detailed Analysis of Block Diagrams: Oral
12. Proposing Technical Solutions: Written
13. Proposing Technical Solutions: Oral
14. **REVIEW – II**

Course Outcomes (COs):

1. Identify a technical problem by performing a comprehensive literature survey. (POs: 1, 2, 3, 4, 5)
2. Compare different solution methods presented in the literature for the technical problem identified. (POs: 1, 2, 3, 4, 5)
3. Predict the impact of various software tools and methods for the identified problem. (POs: 1, 2, 3, 4, 5)
4. Display initial simulation results, showing replication of existing approaches for the identified problem. (POs: 1, 2, 3, 4, 5)
5. Construct a technical block diagram that shows an optimized solution for the identified problem, with respect to existing literature. (POs: 1, 2, 3, 4, 5)

EVALUATION RUBRICS

Criteria	Max Marks	Achievement Levels				CO Mapping
		Inadequate (0 – 33%)	**Developing (34 – 66%)**	**Proficient (67 – 100%)**	**Marks Awarded**	
Introduction to area	**10**	No information about the specific technical details in the chosen area.	Some information about the area, but no clarity in internal details.	Clear presentation of the technical details, internal working, and rationale of design choices.		**CO1, CO2**
Literature Survey	**10**	Very few quality sources pertinent to the chosen technical area. No recent articles used.	Ample sources from recent past, but not from quality sources or with zero or very few citations.	Ample sources from quality journals and conferences recently published, and having abundant citations.		**CO1, CO2**
Problem Statement	**10**	No clear problem identified in chosen area.	Identification of problem area, but no knowledge of underlying technical details.	Clear identification of problem area, along with parameters having an influence on the performance.		**CO3**
Reproduction of Existing Results	**10**	No simulation results shown.	Individual blocks simulated, but no comprehensive simulation.	Complete and consistent reproduction of existing results using appropriate software tools.		**CO4**
Research Questions	**10**	No hypothesis proposed.	Hypothesis is not sound/practical, and not backed by technical arguments.	Sound and practical hypothesis proposed, along with supporting technical/intuitive arguments.		**CO5**
TOTAL MARKS AWARDED						

ANALOG AND MIXED SIGNAL IC DESIGN

Course Code: MVE21 **Credits: 4:0:0**

Prerequisites: Digital and Analog Circuits **Contact Hours: 56**

Course Coordinator: V Anandi

UNIT – I

Single StageAmplifier:CS stage with resistance load, Diode connected load, Current source load, Active load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascode stage, Folded cascode

UNIT – II

Frequency Response of CS Stage: General considerations, Miller effect, Association of poles with nodes, Frequency response of common source stage

Differential Amplifiers and Current Mirrors: Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell, Basic current mirror, Cascode current mirror

UNIT – III

Operational Amplifiers: One stage opamp, Two stage opamp, Gain boosting, Outputswing calculations, Common mode feedback, Input range, Limitations, Slew rate, PSRR, Noise in opamp

Stability and Frequency Compensation: Generalconsiderations, Multipole systems, Phase margin, Basic frequency compensation, Compensation of two-stage opamp

UNIT – IV

Band Gap References and Switched Capacitor Circuits: General considerations, Supply independent biasing, Temperature independent biasing, PTAT current generation, Constant Gm biasing, Sampling switches.

UNIT – V

Data Converter Architecture: DAC and ADC specifications, Qualitative analysis of resistor string DAC, R-2R ladder networks, Current steering DAC,Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC

References:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition,Tata McGraw-Hill, 2018.
2. Douglas R Holberg, Phillip EAllen, "CMOS Analog Circuit Design" 2nd Edition, Oxford University Press, 2013.
3. R.JacobBaker, "CMOS: Circuit Design, Layout, Simulation", Wiley Publications, 2009.
4. Behzad Razavi, "Micro electronics", 1st Edition, Tata McGraw Hill, 2001.

Course Outcomes (COs):

1. Design and analyse current sources/sinks/mirrors and single stage amplifiers. (POs: 1, 3, 4, 5)
2. Analyse the frequency response of the different configurations of an amplifier. (POs: 1, 3, 4, 5)
3. Design and analyse frequency response characteristics of differential amplifier and opamp. (POs: 1, 3, 4, 5)
4. Discuss stability compensation for amplifiers. (POs: 1, 3, 4, 5)
5. Demonstrate proficiency in using VLSI CAD tools for design and analysis of mixed-signal circuits. (POs: 1, 3, 4, 5)

ADVANCED MICROCONTROLLERS

Course Code: MVE22 **Credits: 4:0:0**

Prerequisites: Microcontrollers **Contact Hours: 56**

Course Coordinator: K. V. Suma

UNIT – I

Introduction to ARM Cortex M Processors: What are ARM Cortex M Processors, Advantages of Cortex M Processors, Applications of ARM Cortex M processors, Technical overview, General information, Architecture – Introduction, Programmer's model, Behavior of application programs, Status word, Memory system, Exceptions and interrupts, System control block, Debug, DSP enhancement instructions.

UNIT – II

Instruction Set of ARM Cortex M4: Moving data within the processor, Memory access, Arithmetic operations, Logic operations, Shift and rotate instructions, Data conversion operations, Bit field processing, Compare and test, Program flow control, Saturation operations, Exception-related instructions, Sleep mode-related instructions, Memory barrier instructions

UNIT – III

Low Power and System Control Features of ARM Cortex M4: Low power designs, low power features – sleep modes, system control register, entering sleep mode, wake-up conditions, sleep-on-exit feature, SEVONPEND, Sleep extension/wake-up delay, WIC, Event communication interface, Low power features using WFI and WFE instructions in programming

Cortex M4 Floating Point Unit: Overview, Floating point register overview, CPACR register, Floating point register bank, FPSCR, FPCCR, FPCAR, FPDSCR, Media and floating point feature registers

UNIT – IV

Fault Exceptions and Fault Handling of ARM Cortex M4: Causes of faults, Enabling fault handlers, Fault status registers and fault address registers, Analyzing faults

UNIT – V

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of files generated on cross-compilation, Disassembler/Decompiler, Simulators, Emulators and debugging.

Processor trends in embedded system, embedded OS trends, Development language trends- Java & NET MF, open standards, bottle necks.

References:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M4", 3rd Edition, Newnes, (Elsevier), 2014.
2. Shibu. K. V., "Introduction to Embedded Systems", 2nd Edition, Tata McGraw Hill Education Private Ltd., 2009.
3. David A Patterson, John L Hennessy, "Computer Organization and Design – ARM Edition", 4th Edition, Morgan Kauffman Publishers Elsevier, 2010.

Course Outcomes (COs):

1. Familiarize with the technical overview and architecture of ARM Cortex M4. (POs: 1, 3)
2. Apply the technical knowledge of ARM Cortex M4 to build programs. (POs:1, 3, 4)
3. Illustrate the importance of low power mode and floating point features of ARM Cortex M4. (POs: 1, 3, 4)
4. Identify the causes of failures in ARM Cortex M4 using fault exception mechanism. (POs: 1, 4)
5. Analyze the working of debugger tools for embedded system design and development (POs: 1, 4)

ANALOG AND MIXED SIGNAL IC DESIGN LABORATORY

Course Code: MVEL23 **Credits: 0:0:1**

Prerequisites: Digital and Analog Circuits **Contact Hours: 28**

Course Coordinator: S. L. Gangadharaiah

LIST OF EXPERIMENTS

1. Design the following analog circuits with the given specifications and complete the design flow as mentioned below:
   a. Draw the schematic and perform: DC Analysis, AC Analysis, Transient analysis
   b. Draw the Layout, verify DRC and check for LVS
      (i) CMOS inverter
      (ii) Common source amplifier
      (iii) Common drain amplifier
      (iv) Common gate amplifier
      (v) Differential amplifier
      (vi) Single stage opamp
      (vii) Two stage opamp

2. Design the following digital/mixed signal cicuits and verify the functionality
   (i) 3-8 decoder using MOS technology
   (ii) Two-input OR gate using digital two input NOR gate and analog inverter
   (iii) Two-input NOR gate using analog two input NOR gate and digital inverter
   (iv) Two-input XOR gate using digital two input XNOR gate and analog inverter
   (v) R-2R digital to analog converter

References:

1. Cadence Analog and Mixed Mode Lab Manual, Developed by University Support Team, Cadence, Bangalore, version 3.0, 2014.
2. BehzadRazavi, “Design of Analog CMOS Integrated Circuits”,2nd Edition, Tata McGrawHill, 2018.
3. Phillip E Allen, Douglas R Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 2004.

Course Outcomes (COs):

1. Apply DRC, LVS and different analysis for various single stage amplifiers. (POs: 1, 3, 4, 5)
2. Design the differential amplifier and apply the different analysis, LVS and DRC. (POs: 1, 3, 4,5)
3. Apply DRC, LVS and different analysis for operational amplifiers. (POs: 1, 3, 4,5)
4. Design a DAC and measure different parameters. (POs: 1, 3, 4, 5)
5. Employ mixed signal simulation to OR, NOR and XOR gates. (POs: 1, 3, 4, 5)

ADVANCED MICROCONTROLLERS LABORATORY

Course Code: MVEL24 **Credits: 0:0:1**

Prerequisites: Microcontrollers **Contact Hours: 28**

Course Coordinator: K. V. Suma

LIST OF EXPERIMENTS

1. ARM Cortex M4 assembly programs for data transfer, arithmetic and logic operations
2. C programs on ARM Cortex M4 board for sorting, code conversion and factorial
3. Interfacing programs for ARM Cortex M4 with
   - (i) Display (LCD & LED) modules
   - (ii) 16 channel 8 bit ADC
   - (iii) DC motor speed control and measurement
   - (iv) Generation of sine and square waveforms using Dual DAC
   - (v) Elevator
   - (vi) Calculatortype keyboard
   - (vii) Relay output
   - (viii) Real time clock
   - (ix) Stepper motor
   - (x) Temperature sensor monitoring and control

References:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex M4", 3rd Edition, Newnes, (Elsevier), 2014.

Course Outcomes (COs):

1. Employ simulation and emulation IDE. (POs: 4, 5)
2. Write, compile and debug assembly language and C programs for ARM Cortex M4. (POs: 1, 3, 5)
3. Implement C programs to interface display modules and data converters to ARM Cortex M4 microcontroller. (POs: 1, 4, 5)
4. Develop C programs to control DC motor, stepper motor and relay through ARM Cortex M4 microcontroller. (POs: 1, 4, 5)
5. Implement C programs to interface keyboard, RTC and temperature sensor modules to ARM Cortex M4 microcontroller. (POs: 1, 4, 5)

TECHNICAL SEMINAR – II

Course Code: MVE25 **Credits: 0:0:2**

Prerequisites: Nil **Contact Hours: 56**

LIST OF ACTIVITIES

1. Detailed discussion of block diagrams
2. Setting up the simulation environment
3. Simulation of results
4. Reproduction of simulation results: Written
5. Presentation of simulation results: Oral
6. Proposing a technical block diagram: Written
7. Proposing a technical block diagram: Oral
8. **REVIEW – 1**
9. Design of Experiments
10. Design of Experiments
11. Presentation of simulation results: Written
12. Presentation of simulation results: Oral
13. Comprehensive report writing
14. **REVIEW – 2**

Course Outcomes (COs):

1. Present initial simulation results, replicating existing findings. (POs: 1, 2, 3, 4, 5)
2. Propose a technical block diagram with arguments for improved performance. (POs: 1, 2, 3, 4, 5)
3. Enumerate the tools required for performing experiments, and justify their appropriateness. (POs: 1, 2, 3, 4, 5)
4. Discuss simulation results and optimized performance metrics. (POs: 1, 2, 3, 4, 5)
5. Compare the advantages and disadvantages of approach, along with possible future directions. (POs: 1, 2, 3, 4, 5)

EVALUATION RUBRICS

Criteria	Max Marks	Achievement Levels				CO Mapping
		Inadequate (0 – 33%)	**Developing (34 – 66%)**	**Proficient (67 – 100%)**	**Marks Awarded**	
Reproduction of existing results	**10**	Partial reproduction of results or large variation from reported results, no proper presentation using tables etc.	Partial reproduction of results, but no proper presentation and no analysis.	Complete reproduction of results, with appropriate tables/figures and analysis of results obtained.		**CO1**
Proposed Approach	**10**	No proper justification for methods used, or no new methods proposed.	New approach proposed, but without any justification.	New approach proposed, along with technical arguments that support the hypothesis.		**CO2**
Tool usage	**10**	Tool usage is not appropriate, is incorrect, or is incomplete.	Tools are used appropriately, but without knowledge of advanced options.	Tools are used appropriately, with complete knowledge of all available settings options suitable for analysis.		**CO3**
Results	**10**	Results are not indicative of proposed model, or are incomplete.	Results are complete, but are not better than existing solutions. Proper formats are used for presentation.	Results are presented using appropriate formats, and are better than existing solutions for the problem identified.		**CO4**
Discussion & Conclusions	**10**	No discussion of experiments and the results obtained.	Summary of experiments and results obtained thereby.	Summary of experiments and results obtained thereby, along with conclusions and future directions.		**CO5**
TOTAL MARKS AWARDED						

LOW POWER VLSI DESIGN

Course Code: MVE31 **Credits: 4:0:0**

Prerequisites: CMOS VLSI Circuits **Contact Hours: 56**

Course Coordinator: V. Anandi

UNIT – I

Power Dissipation in CMOS: Introduction, Need for low power VLSI chips, Sources of power consumption, Introduction to CMOS inverter power dissipation, Low power VLSI design limits

UNIT – II

Logical Level Power Optimization: gate reorganization, local restructuring, signal gating, logic encoding, state machine encoding, pre-computation logic

Circuit Level Power Optimization: Transistor and gate sizing, Equivalent pin ordering, Network restructuring and re-organization, Special latches and flip-flops

UNIT – III

Low Power Memory Design: Sources of power dissipation in DRAM and SRAM, Low power techniques for SRAM, Low power DRAM circuits, Special techniques: power reduction and clock networks, low power bus, delay balancing

UNIT – IV

Power Estimation: Simulation power analysis: SPICE circuit simulation, Gate level simulation, Architectural level analysis, Data correlation analysis in DSP systems, Monte-Carlo simulation. Probabilistic power analysis: random signals, probabilistic techniques for signal activity estimation, propagation of static probability in logic circuits, gate level power analysis using transition density

UNIT – V

Synthesis and Software Design for Low Power: Synthesis for low power: behavioral level transforms, algorithm level transforms for low power, architecture driven voltage scaling, power optimization using operation reduction, operation substitution, Software design for low power: gate level, architecture level, bus switching activity

References:

1. Gary Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic Publishers, 2002.
2. K. Roy, S. C. Prasad, “Low Power CMOS VLSI Circuit Design”, Indian Edition 2008, Wiley, 2000,
3. Jan M. Rabaey, Massoud Pedram, “Low Power Design Methodologies”, KAP, 1996.
4. A. P. Chandrakasan, R.W. Broadersen, “Low Power Digital CMOS Design”, Kluwer, 1995

Course Outcomes (COs):

1. Recall fundamental low power design concepts to classify power dissipation mechanisms in CMOS ICs. (POs: 1, 4)
2. Classify various power optimization techniques at circuit and logic level. (POs: 1, 4)
3. Design special circuits like clock generator, memories with special reference to speed and power consumption. (POs: 1, 3, 4)
4. Differentiate between various power measurement and estimation techniques at different levels of abstraction. (POs: 1, 4)
5. Analyze different architectural level low power transforms and logic synthesis techniques for DSP filters. (POs: 1, 3, 4)

INTERNSHIP/INDUSTRIAL TRAINING

Course Code: MVE32 **Credits: 0:0:4**

Prerequisites: Nil

The evaluation of students will be based on an intermediate presentation, along with responses to a questionnaire testing for outcomes attained at the end of the internship. The rubrics for evaluation of the presentation and the questionnaire for the report will be distributed at the beginning of the internship.

Course Outcomes (COs):

1. Analyze the working of complex technical systems/blocks. (POs: 1, 3, 4)
2. Appreciate the use and impact of modern tools on the engineering design cycle. (POs: 1, 3, 4)
3. Participate effectively as a member of a team under the supervision of a manager/mentor. (POs: 5)
4. Understand the importance of professional and ethical behavior in the engineering workplace. (POs: 1, 3, 4)
5. Appreciate the requirements for constant technology updation. (POs: 1, 3, 4)

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Complex Technical Blocks	**10**	No working knowledge of the domain.	Working knowledge of the domain, with some knowledge of internal details.	Detailed understanding of the system, along with underlying mechanisms.		**CO1**
Error Debugging	**10**	No ability to diagnose or correct errors, or improve performance.	An ability to diagnose errors, but not correct them, no intuition on improving performance.	Diagnose and correct erroneous system operation, and propose methods to improve system performance.		**CO2**
Professional and Ethical Behavior	**10**	No knowledge of the requirement of professional and ethical behavior.	Understands the requirement for professional and ethical behavior.	Can predict the effects of non-professional an un-ethical behavior in the workplace.		**CO3**
Engineering and Finance	**10**	Cannot make the connection between engineering decisions and their economic impact.	Predict the cost of engineering decisions.	Creates designs keeping their economic impact in mind.		**CO4**
Lifelong Learning	**10**	No understanding of the requirements for lifelong learning in the engineering profession.	Can present examples of the impact of lifelong learning in the engineering industry.	Can present examples of the impact of lifelong learning, along with predicting future areas of impact of life-long learning.		**CO5**
TOTAL MARKS AWARDED						

PROJECT WORK – I

Course Code: MVE33 **Credits: 0:0:6**

Prerequisites:--

The students will be evaluated based on two oral presentations during the semester. In the presentations they will have to discuss the results of their literature survey and initial implementations of the design.

Course Outcomes (COs):

1. Choose recent literature published in quality journals, and discuss the implementation details and results obtained therein. (POs: 1, 2, 3, 4, 5)
2. Formulate precise, accurate, and unambiguous objectives for the project, based on study of the literature. (POs: 1, 2, 3, 4, 5)
3. Develop a detailed methodology for achieving the objectives identified for the project, including technical blocks and implementation platforms. (POs: 1, 2, 3, 4, 5)
4. Generate technical documents recording the tasks performed, adhering to professional standards. (POs: 1, 2, 3, 4, 5)
5. Present orally the tasks performed, using appropriate visual and explanatory aids. (POs: 1, 2, 3, 4, 5)

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels Phase – I, Review – I				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Introduction	**5**	Introduction is not clear, or is not technically accurate.	Introduction is accurate, but no in-depth analysis of the domain.	Clear introduction to the domain, along with design decisions and their impacts.		**CO1**
Literature survey	**10**	Few sources of low quality, with no proper discussion of results.	Appropriate discussion of existing results, but quality of sources is low.	Comprehensive list of results presented from recent quality sources.		**CO2**
Methods comparison	**5**	Methods not explained and compared in terms of internal implementation details.	Advantages and disadvantages discussed, but not with reference to actual methods.	Detailed description of existing methods, along with their advantages and disadvantages.		**CO3**
TOTAL MARKS AWARDED						

Criteria	Max. Marks	Achievement Levels Phase – I, Review – II				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Methods discussion	**10**	No implementation level discussion of methods used in literature.	Brief discussion of tools used and results obtained therein.	Detailed discussion of tools used and their impact on the quality of results obtained in literature sources.		**CO3**
Initial Results	**10**	Initial results are not complete, or do not match that of existing literature.	Proper tools used to generate results, but are not same as existing literature.	Suitable tools used with appropriate conditions to generate initial results, and a discussion of the latter.		**CO4**
Technical Block Diagram	**10**	Technical block diagram proposing improvements is not technically justified.	Block diagram proposing improvements is technically justified.	Multiple block diagrams for optimization are presented, with a detailed analysis of the advantages and disadvantages of each approach.		**CO5**
TOTAL MARKS AWARDED						

PROJECT WORK – II

Course Code: MVE41 **Credits: 0:0:22**

Prerequisites:--

The students will be evaluated based on two oral presentations, in which they will present their proposed solutions to the problem identified, and discuss the implementation details and results obtained.

Course Outcomes (COs):

1. Determine the scope of the study by choosing appropriate assumptions and selecting measurable benchmarks for judging progress/outcomes. (POs: 1, 2, 3, 4, 5)
2. Design a suitable set of experiments that is capable of comprehensively testing the hypotheses proposed as part of this study. (POs: 1, 2, 3, 4, 5)
3. Analyze the results obtained, discuss their validity, and their support of hypotheses proposed. (POs: 1, 2, 3, 4, 5)
4. Generate technical documents recording the tasks performed, adhering to professional standards. (POs: 1, 2, 3, 4, 5)
5. Present orally the tasks performed, using appropriate visual and explanatory aids. (POs: 1, 2, 3, 4, 5)

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels Phase – II, Review – I				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Technical Block Diagram	**10**	A discussion of methods for optimization is not based on technical arguments.	One or more block diagrams presented for optimization, but not justified with technical arguments.	One or more block diagrams presented for optimization, along with along with accurate technical arguments for justification.		**CO1**
Initial Results	**10**	Results are not matching expectations, or are not complete.	Complete results generated, but not an improvement on existing metrics.	Complete results generated with an improvement over existing approaches due to proposed block diagram.		**CO2**
TOTAL MARKS AWARDED						

Criteria	Max. Marks	Achievement Levels Phase – II, Review – II				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Design of Experiments	**10**	Few experiments conducted, with no relation to problem domain.	Significant experiments conducted, but with no structure and relation to problem domain.	Significant experiments conducted, with all relevant parameters being tested in an orderly manner, and with relevance to hypothesis.		**CO3**
Experimental Results	**10**	Few results, not covering all cases, and not optimizing performance.	Performance is moderately optimized with respect to existing approaches, but not to the level predicted by block diagram.	Significant improvement in results, matching predictions in technical block diagram.		**CO4**
Discussion& Future Work	**10**	No qualitative or quantitative discussion of the method, and its key characteristics.	Method is discussed, but without arguments justifying the advantages and disadvantages of the approach.	Method is summarized in detail, along with technical arguments justifying the advantages and disadvantages of the proposed method.		**CO5**
TOTAL MARKS AWARDED						

ELECTIVES

ADVANCED EMBEDDED SYSTEMS

Course Code: MVEE01 **Credits: 4:0:0**

Prerequisites: Embedded Systems **Contact Hours: 56**

Course Coordinator: K. V. Suma

UNIT – I

Typical Embedded System: Core of embedded system, Memory, Sensors and actuators, Embedded firmware, Other system components. Characteristics and quality attributes of embedded systems

UNIT – II

Embedded System Design and Development: System design and development, Life-cycle models –Waterfall model, V cycle model, Spiral model and Rapid Prototyping incremental, problem solving – five steps to design, design process, identifying the requirements, formulating the requirements specifications, system design specification, system specifications vs system requirements

Hardware Software Co-Design and Program Modeling: Fundamental issues in hardware software co-design, Computational models in embedded design

UNIT – III

Embedded Hardware Design and Development: EDA tools, How to use EDA tool, Schematic design – Place wire, Bus, Port, Junction, Creating part numbers, Design rules check, Bill of materials, Netlist creation, PCB layout design – Building blocks, Component placement, PCB track routing

Embedded Firmware Design and Development: Embedded firmware design approaches, Embedded firmware development languages

UNIT – IV

Software Modeling: Introduction to UML, UML diagrams, Use cases, Class diagrams, Dynamic modeling with UML, Interaction diagrams, Sequence diagrams, Fork and join, Branch and merge, Activity diagram, State chart diagrams, Dynamic modeling with structural design methods

UNIT – V

Real Time Operating Systems (RTOS) based Embedded System Design: Operating system basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Threads, Processes and Scheduling: Putting them altogether, Task communication, Device drivers, How to choose an RTOS

References:

1. Shibu K V, "Introduction to Embedded Systems", 2nd Edition, Tata McGraw Hill Education Private Limited, 2009.
2. James K Peckol, "Embedded Systems – A Contemporary Design Tool", 4th Edition, John Wiley, 2008.

Course Outcomes (COs):

1. Identify the basic building blocks, characteristics and quality attributes of embedded systems. (POs: 1, 4)
2. Analyze the complete life cycle of embedded system design and development. (POs: 3, 4)
3. Design a printed circuit board for a given circuit by using PCB design IDE. (POs: 1, 3, 4)
4. Interpret the various computational models of software in embedded system design. (POs: 1, 4)
5. Select the RTOS for real time embedded system design. (POs: 1, 3, 4)

DIGITAL SYSTEM DESIGN USING HDL

Course Code: MVEE02 **Credits: 4:0:0**

Prerequisites: Digital Electronics **Contact Hours: 56**

Course Coordinator: S. L. Gangadharaiah

UNIT – I

Introduction and Methodology: Digital systems and embedded systems, Binary representation and circuit elements, Real world circuits, Models, Design methodology

Number Basics: Unsigned and signed integers, Fixed and floating point numbers

UNIT – II

Sequential Basics: Storage elements, Counters, Sequential data paths and control, Clocked synchronous timing methodology

UNIT – III

Memories and Implementation Fabrics: Concepts, Memory types, Error detection and correction, ICs, PLDs, Packaging and circuit boards, Interconnection and signal integrity

UNIT – IV

System Verilog Simulation and Synthesis: System Verilog extension to Verilog, RTL and gate level modeling, RTL synthesis, Subset of System Verilog, System Verilog simulation, Digital synthesis, Modules, Procedural blocks

UNIT – V

RTL Modeling Fundamentals: System Verilog language rules – Module, Module instances, Hierarchy, Four state data values, Data types, Variable types, Net types, Operators, Continuous signal assignments, Procedural signal assignments, Modeling combinational logic and sequential logic

References:

1. Peter J. Ashenden, “Digital Design: An Embedded Systems Approach using Verilog”, Elsevier, 2010.
2. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, 2nd Edition, Pearson Education, 2010.

3. Stuart Sutherland, “RTL Modeling with System Verilog for Simulation and Synthesis: Using System Verilog for ASIC and FPGA Design”, 1st Edition, Create Space Independent Publishing Platform, 2017.
4. Chris Spear, Greogory J Tumbush, “System Verilog for Verification – A Guide to Learning Test Bench Language Features”, Springer, 2012.

Course Outcomes (COs):

1. Apply the concepts of Verilog modeling to design and verify the operations of complex digital logic circuits. (POs: 1, 3, 4)
2. Design, model and test pipelined storage elements, sequential data path controllers based on signed, unsigned fixed point and floating point number systems with Verilog. (POs:.1,3,4)
3. Employ Verilog modeling to multi-port memories, FIFO data paths and FSMs with respect to integrated circuits. (POs: 1, 3, 4)
4. Illustrate the basics of System Verilog to simulate and synthesize digital systems. (POs: 1, 3, 4)
5. Design and model combinational and sequential circuits using System Verilog. (POs: 1, 3, 4)

DIGITAL VLSI TESTING

Course Code: MVEE03 **Credits: 4:0:0**

Prerequisites: Digital System Design using HDL **Contact hours: 56**

Course Coordinator: Deepali B Koppad

UNIT – I

Introduction: Role of testing, Testing during the VLSI life cycle, Challenges in VLSI testing, test economics, Yield, Fault coverage, Historical review of VLSI test technology

Fault Modeling: Various fault models, Single Stuck-at fault – fault equivalence, fault collapsing

UNIT – II

Logic and Fault Simulation: Simulation models, Algorithms for true value simulation, Algorithms for fault simulation, Statistical methods for fault simulation

Testability Measures: Controllability and Observability, SCOAP testability analysis, Simulation based testability analysis, RTL testability analysis

UNIT – III

Combinational Circuit Test Generation: ATPG algebras, Combinational ATPG Algorithms – Naïve example, D-Algorithm, PODEM, FAN

DFT and Scan Design: Ad-Hoc DFT, Scan based design

UNIT – IV

Sequential Circuit Test Generation: Time frame expansion method, Simulation-based sequential ATPG

Logic BIST: Test pattern generation, output response analyzer, BIST architectures, Fault coverage enhancement, Memory Testing.

UNIT – V

Boundary Scan: Introduction and motivation, TAP controller and port, SOC test problems

Testing in the Nanometer range: Delay testing, Physical failures and soft errors, High-speed I/O testing

References:

1. Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, “VLSI Test Principles and Architectures: Design for Testability”, Morgan Kaufmann Publishers, 2006.
2. Michael L. Bushnell, Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, “Digital Systems Testing and Testable Design”, Wiley – IEEE Press, 1993.

Course Outcomes (COs):

1. Create and manipulate fault models of VLSI circuits. (POs: 1, 3, 4)
2. Perform fault simulations, and predict testability measures of digital circuits. (POs: 1, 3, 4)
3. Generate optimized test patterns for combinational and sequential logic circuits. (POs: 1, 3, 4)
4. Design scan chains and BIST modules for digital designs. (POs: 1, 3, 4)
5. Employ boundary scan elements in design. (POs: 1, 3, 4)

ADVANCED DIGITAL LOGIC VERIFICATION

Course Code: MVEE04 **Credits: 4:0:0**

Prerequisites: Digital System Design using HDL **Contact Hours: 56**

Course Coordinator: S. L. Gangadharaiah

UNIT – I

Verification Concepts: Concepts of verification, Importance of verification, Stimulus vs Verification, Test bench generation, Functional verification approaches, Typical verification flow, Stimulus generation, Direct testing, Coverage: Code coverage and functional coverage, Coverage plan

UNIT – II

System Verilog – Language Constructs: Data types: Two state data, Strings, Arrays: Queues, Dynamic and associative arrays, Structs, Enumerated types. Program blocks, modules, interfaces, Clocking ports, Mod ports

UNIT – III

System Verilog – Classes and Randomization: SV classes, Language evolution, Classes and objects, Class variables and methods, Class instantiation, Inheritance and encapsulation, Polymorphism, Randomization: Directed vs Random testing, Randomization: Constraint driven randomization

UNIT – IV

System Verilog – Assertions and Coverage: Assertions: Introduction to assertion based verification, Immediate and concurrent assertions, Coverage driven assertion: Motivation, types of coverage, Cover group, Cover point, Cross coverage, Concepts of binning and event sampling

UNIT – V

Building Test Bench: Layered test bench architecture, Introduction to Universal Verification Methodology (UVM), Overview of UVM, Base classes and simulation phases in UVM and UVM macros, Unified messaging in UVM, UVM environment structure, Connecting DUT-virtual interface

References:

1. System Verilog 3.1a LRM, Accellera's Extensions to Verilog.
2. Chris Spear, Greogory J Tumbush, "System Verilog for Verification – A Guide to Learning Test Bench Language Features", Springer, 2012.
3. SasanIman, "Step by Step Functional Verification with System Verilog and OVM", Hansen Brown Publishing, 2008.
4. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design – A Guide to using System Verilog for Hardware Design and Modeling", 2nd Edition, Springer Publications, 2006.
5. Janick Bergeron, "Writing Test Benches using System Verilog", Springer International Edition, 2009.
6. www.asic-world.com
7. www.testbench.in

Course Outcomes (COs):

1. Discuss the principle and importance of verification. (POs: 1, 3, 4)
2. Apply OOPs concepts in System Verilog to verify a digital system. (POs: 1, 3, 4)
3. Develop basic verification environment using System Verilog. (POs: 1, 3, 4)
4. Create random stimulus and track functional coverage using System Verilog. (POs: 1, 3, 4)
5. Illustrate the concepts of layered test bench architecture and its components. (POs: 1, 3, 4)

MEMS AND NANOELECTRONICS

Course Code: MVEE05 **Credits: 4:0:0**

Prerequisites: Semiconductor Theory **Contact Hours: 56**

Course Coordinator: Lakshmi. S

UNIT – I

Introduction to MEMS: Feynman's vision, Multi-disciplinary aspects, Application areas, Scaling laws in miniaturization, scaling in geometry, scaling in rigid body dynamics, electrostatics and electromagnetics, Electrical fluid flow.

Micro and Smart Devices and Systems: Principles: Transduction principles in MEMS Sensors: Actuators: different actuation mechanisms – silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, silicon micro-mirror arrays, piezo-electric based inkjet print head, electrostatic comb-driver

UNIT – II

Micromanufacturing and Packaging: Lithography, thin-film deposition, etching (wet and dry), etch stop techniques, wafer-bonding, Silicon micromachining: surface, bulk, LIGA process.

Integration and Packaging of MEMS devices: Integration of microelectronics and micro devices at wafer and chip levels, Microelectronic packaging: wire and ball bonding, flipchip.

UNIT – III

Electrical and Electronic Aspects of MEMS: Coupled electro mechanics, stability and Pull-in phenomenon, Practical signal conditioning circuits for microsystems, RF MEMS: Switches, varactors, tuned filters

UNIT – IV

Introduction to Nanoelectronics: Particles and waves, Wave-particle duality, Wave mechanics, Schrödinger wave equation, Electrons in traditional low-dimensional structures, Electrons in quantum wells, Electrons in quantum wires, Electrons in quantum dots, Nanostructure devices, Resonant tunneling diodes, Single-electron-transfer devices

UNIT – V

Fabrication and Measurement Techniques for Nanostructures: Bulk crystal and hetero structure growth, Nanolithography

Measurement and Applications of Nano devices: Techniques for characterization of nanostructures, Injection Lasers: Quantum cascade lasers, Single photon sources, Biological tagging, Optical memories, Coulomb blockade devices, Photonic structures

References:

1. G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat, V.K. Aatre, "Micro and Smart Systems", Wiley India, First edition, 2010.
2. T R Hsu, "MEMS and Microsystems Design and Manufacturing", 2nd Tata McGraw Hill, Edition, 2008.
3. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications", Cambridge University Press, 2011.
4. George W. Hanson, "Fundamentals of Nanoelectronics", Pearson Education India, 2009.
5. Charles P. Poole, Jr, Frank J. Owens, "Introduction to Nanotechnology", John Wiley & Sons, 2003

Course Outcomes (COs):

1. Analyze scaling laws and operation of various practical MEMS. (POs: 1,3)
2. Describe various fabrication techniques and packaging methods for MEMS devices. (POs: 1, 3)
3. Identify the electronics and RF aspects of MEMS. (POs: 3,4)
4. Recognize the distinguishing aspect of nanoscale devices and systems. (POs: 3, 4)
5. Examine design, fabrication and characterizationof nanoscale systems and their applications. (POs: 3, 4)

MACHINE AND DEEP LEARNING

Course Code: MVEE06 **Credits: 4:0:0**

Prerequisites: Advanced Engineering Mathematics **Contact Hours: 56**

Course Coordinator: S. Sethu Selvi

UNIT – I

Introduction: What is machine learning, Example machine learning applications

Supervised Learning: Learning a class from examples, VC dimension, PAC learning, Noise, Learning multiple classes, Regression, Model selection and generalization

Bayesian Decision Theory: Classification, Losses and Risks, Discriminant functions, Association rules

UNIT – II

Parametric Methods: Maximum likelihood estimation, Evaluating an estimator, Bayes estimator, Parametric classification, Regression, Tuning model capacity

Dimensionality Reduction: Subset Selection, Principal Component Analysis (PCA), SVD and Matrix factorization, Linear Discriminant Analysis (LDA)

UNIT – III

Unsupervised Learning: Clustering:k–Means Clustering, EM algorithm, Hierarchical Clustering, Decision Trees: Univariate and Multivariate trees

UNIT – IV

Multilayer Perceptrons: Perceptron, Training a perceptron, Learning Boolean functions, Multilayer perceptrons, Backpropagation algorithm, Training procedures, Dimensionality reduction, Deep learning

Deep Neural Networks: Deep feed forward networks, regularization for deep learning

UNIT – V

Deep Neural Networks: Optimization for training deep models, convolutional networks

Sequence Modeling: Recurrent and Recursive nets, LSTM, Gated RNNs, Practical methodology, Applications

References:

1. EthemAlpaydin, "Introduction to Machine Learning", 3rd Edition, PHI Learning Pvt. Ltd, 2015.
2. Ian Goodfellow, YoshuaBengio, Aaron Courville, "Deep Learning", MIT Press, 2017.
3. Christopher Bishop, "Pattern Recognition and Machine Learning", CBS Publishers & Distributors, 2010
4. Tom Mitchell, "Machine Learning", McGraw Hill, 1997.
5. Michael Nielsen, "Neural Networks and Deep Learning", 2019.

Course Outcomes (COs):

1. Examine the concepts of various supervised learning algorithms and employ bayesian learning for classification (POs – 1, 3, 4)
2. Evaluate parametric methods for classification and investigate various dimensionality reduction algorithm (POs – 1, 3, 4)
3. Analyse unsupervised learning algorithms and multivariate concepts (POs – 1, 3, 4)
4. Appreciate the concepts of deep learning and apply deep feed forward network practical problems (POs – 1, 3, 4)
5. Apply convolutional networks and demonstrate how recurrent and recursive nets function can be mapped to practical applications (POs – 1, 3, 4)

INTERNET OF THINGS (IoT)

Course Code: MVEE07 **Credits: 4:0:0**

Prerequisites: Computer Networks **Contact Hours: 56**

Course Coordinator: Suma K V

UNIT – I

Introduction: Definition and characteristics of IoT, Things in IoT, IoT protocols, IoT functional blocks, IoT communication models, IoT communication APIs, IoT enabling technologies, IoT levels and deployment templates, IoT and M2M, SDN and NFV for IoT, IoT system management with NETCONFIG – YANG

UNIT – II

Developing Internet of Things: IoT platform design methodology, Specifications: Requirements, Process, Domain, Information, Services, Level, Functional, Operational, Integration, Application development

Python Language: Data types and data structures, Control flow, Functions, Modules, Packages, File handling, Date and time operations, Classes, Python packages of interest for IoT

UNIT – III

IoT Physical Devices and End Points: Basic building blocks of an IoT Device, Raspberry Pi, Linux on Raspberry Pi, Raspberry Pi Interfaces: Serial, SPI, I2C

Programming Raspberry Pi with Python: Controlling LED, Interfacing switch, Interfacing light sensor

UNIT – IV

Cloud and Data Analytics: Introduction to cloud storage models and communication APIs

Web Application Framework: Django, Web Services for IoT, SkyNet messaging platform, Data analytics for IoT, Apache: Hadoop, Oozie, Storm, Real time data analysis, Tools for IoT

UNIT – V

IoT Case Studies: Home automation: Smart lighting, Home intrusion detection, Cities: Smart parking environment: Weather monitoring system, Weather reporting bot, Air pollution monitoring, Forest fire detection; Agriculture – Smart irrigation, IoT printer, IoT in automobiles: Intelligent transportation and connected vehicle, Vehicular Ad-hoc Networks (VANETs)

References:

1. Arshdeep Bahga, Vijay Madisetti, "Internet of Things: A Hands-on Approach", University Press, 2015.
2. Pethuru Raj, Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases Description", Taylor & Francis, CRC Press, 2017.
3. Daniel Minoli, "Building the Internet of Things with IPv6", John Wiley & Sons, 2013.

Course Outcomes (COs):

1. Describe the OSI Model for the IoT/M2M systems. (POs: 1, 3)
2. Learn basics of design, integration and applications of IoT models. (POs: 1, 3)
3. Acquire the knowledge of basic blocks of IoT devices using Raspberry Pi. (POs: 3)
4. Elaborate on cloud storage models and web services for IoT. (POs: 3)
5. Appraise with various case studies. (POs: 1, 3, 4)

PHYSICS OF SEMICONDUCTOR DEVICES

Course Code: MVEE08 **Credits: 4:0:0**

Prerequisites: Solid State Devices and Circuits **Contact Hours: 56**

Course Coordinator: Raghuram S

UNIT – I

Energy Bands and Charge Carriers in Semiconductors: Bonding forces in solids, Energy bands, Metals, Semiconductors, Insulators, Electrons and Holes, Effective mass, Fermi Level, Electron and hole concentrations in equilibrium

UNIT – II

Conductivity and Mobility: Effects of temperature and doping on mobility, Hall effect, Carrier lifetime, Direct and indirect recombination, Diffusion and drift of carriers, Continuity equation, Steady state carrier injection

UNIT – III

PN Junctions: Contact potential, Fermi levels and space charge, Junction current, Carrier injection, Time variation of stored charge, Capacitance of PN junctions, Schottky barriers, Rectifying and ohmic contacts, Heterojunctions

UNIT – IV

Bipolar Junction Transistors: Fundamental operation, Amplification, Terminal currents, Cutoff and saturation, Secondary effects, Gummel Poon model, Capacitance and charging time, Heterojunction bipolar transistors

UNIT – V

MOS Capacitor and Threshold Voltage: MOSFET: Output and transfer characteristics, Short channel I-V model, Control of threshold voltage, Substrate bias effect, Subthreshold characteristics, Equivalent circuit, Secondary effects, Advanced MOSFET structures

References:

1. Ben Streetman, Sanjay Bannerjee, “Solid State Electronic Devices”, 7th Edition, Prentice Hall India, 2014.
2. Robert F Pierret, “Semiconductor Device Fundamentals”, 2nd Edition, Addison Wesley, 1996.

3. Robert F Pierret, “Advanced Semiconductor Fundamentals”, 2nd Edition, Prentice Hall, 1992.

Course Outcomes (COs):

1. Estimate carrier concentration in semiconductors, given the type and doping level of impurities. (POs: 3, 4)
2. Predict drift and diffusion carrier concentration in semiconductors. (POs: 3, 4)
3. Compute the current through a PN junction, under forward and reverse biased conditions. (POs: 3, 4)
4. Apply basic and advanced electronic concepts to derive models for current flow in a BJT transistor. (POs: 3, 4)
5. Employ electronic concepts to predict qualitative and quantitative operating conditions of MOS transistors. (POs: 3, 4)

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

Course Code: MVEE09 **Credits: 4:0:0**

Prerequisites: Digital Electronic Circuits **Contact Hours: 56**

Course Coordinator: S.L. Gangadhariah

UNIT – I

Introduction to Synthesis and Optimization: Design of microelectronics circuits, Computer aided synthesis and optimization

Hardware Modeling: Abstract models, Compilation and behavioral optimization

UNIT – II

Graph Theory for CAD: Graphs, Combinatorial optimization, Graph optimization problems and algorithms, Boolean algebra and applications

Architectural Synthesis and Optimization: Fundamental architectural synthesis problems, Area and performance estimation, Strategies for architectural optimization, Data path synthesis, Control path synthesis

UNIT – III

Two Level Combinational Logic Optimization: Introduction, Logic optimization, Operations on two level logic covers, Algorithms for logic minimization, Symbolic minimization and encoding problems, Minimization of boolean relations

UNIT – IV

Multiple Level Combinational Logic Optimization: Introduction, Models and transformations for combinational networks, Algebraic model, Boolean model

Sequential Logic Optimization: Introduction, Sequential logic optimization using state based models, Sequential logic optimization using network models, Implicit FSM traversal methods

UNIT – V

Scheduling Algorithms: Introduction, A model for scheduling problems, Scheduling with resource constraints, Scheduling without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling pipelined circuits

Resource Sharing and Binding: Sharing and binding for resource dominated circuits, Sharing and binding for general circuits, Concurrent binding and scheduling, Resource sharing and binding for non-scheduled sequencing graphs

References:

1. Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw Hill, 2003.
2. Edwars M. D., "Automatic Logic Synthesis Techniques for Digital Systems", Macmillan New Electronic Series, 1992.

Course Outcomes (COs):

1. Appreciate the top down approach in design of digital circuits. (POs: 1, 3, 4)
2. Apply the concepts of graph theory in optimization of boolean equations. (POs: 1, 3, 4)
3. Implement different two-level logic optimization algorithms for combinational circuits. (POs: 1, 3, 4)
4. Employ multilevel and sequential optimization algorithms to build digital circuits. (POs: 1, 3, 4)
5. Illustrate different scheduling algorithms with and without resource binding for pipelined sequential circuits. (POs:1, 3, 4)

ASIC DESIGN

Course Code: MVEE10 **Credits: 4:0:0**

Prerequisites: CMOS VLSI Circuits **Contact Hours: 56**

Course Coordinator: V. Anandi

UNIT – I

Introduction to ASICs: Full custom, Semi-custom and programmable ASICs, ASIC design flow, ASIC cell libraries

CMOS Logic: Data path logic cells**:** Data path elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path operators, I/O cells

UNIT – II

ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages

Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT 2 and ACT3 logic modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX

UNIT – III

Programmable ASIC I/O Cells: Xilinx and Altera I/O block

Low-level Design Entry: Schematic entry: Hierarchical design, Netlist screener

ASIC Construction: Physical design, CAD tools

Partitioning: Goals and objectives, Constructive partitioning, Iterative partitioning improvement, KL and look ahead algorithms

UNIT – IV

Floor Planning and Placement: Goals and objectives, Floor planning tools, Channel definition, I/O and power planning and clock planning

Placement: Goals and objectives, Min-cut placement algorithm, Iterative placement improvement, Physical design flow

UNIT – V

Routing: Global routing: Goals and objectives, Global routing methods, Back-annotation

Detailed Routing: Goals and objectives, Measurement of channel density,Left-Edge and Area-Routing Algorithms. Special routing, Circuit extraction and DRC

References:

1. M J S Smith, “Application Specific Integrated Circuits”, Pearson Education, 2003.
2. Neil H. E. Weste, David Harris, Ayan Banerjee, “CMOS VLSI Design: A Circuits and Systems Perspective”, 3rd Edition, Addison Wesley/Pearson Education, 2011.
3. Vikram Arkalgud Chandrasetty, “VLSI Design: A Practical Guide for FPGA and ASIC Implementations”, Springer, 2011.
4. Rakesh Chadha, J. Bhasker, “An ASIC Low Power Primer: Analysis, Techniques and Specification”, Springer Publications, 2015.

Course Outcomes (COs):

1. Describe the concepts of ASIC design methodology, data path elements and FPGA architectures. (POs: 3, 4)
2. Design data path elements for ASIC cell libraries and compute optimum path delay. (POs: 3, 4)
3. Employ industry synthesis tools to achieve desired objectives. (POs: 1, 2, 3, 5)
4. Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and physical design flow. (POs: 1, 3, 4)
5. Create floor plan including partition and routing using CAD algorithms. (POs: 3, 4)

SYSTEM ON CHIP DESIGN

Course Code: MVEE11 **Credits: 4:0:0**

Prerequisites: CMOS VLSI Circuits **Contact Hours: 56**

Course Coordinator: A. R. Priyarenjini

UNIT – I

Motivation for SOC Design: Review of Moore's law and CMOS scaling, Benefits of system-on-chip integration in terms of cost, power, and performance, Comparison of System-on-Board, System-on-Chip, and System-in-Package, Typical goals in SOC design – cost reduction, power reduction, design effort reduction, performance maximization

UNIT – II

Application Specific Integrated Circuits (ASIC): Overview of ASIC types, Design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SOC design methodologies, Application specific Instruction Processor (ASIP) concepts

UNIT – III

No Instruction Set Computer (NISC): No instruction set computer **(**NISC) Control words methodology, NISC application and advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction-set Processors (ASIP), No-Instruction-set-computer (NISC) design flow, Modeling NISC architectures and systems, Use of generic netlist representation

UNIT – IV

Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, Design of verification vectors, Low power FPGA, Reconfigurable systems, SOC related modeling of data path design and control logic, Minimization of interconnect impact, clock tree issues

UNIT – V

Low Power SOC Design/Digital system: Design synergy, Low power system perspective – power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), Building block optimization, Building block memory, Power down techniques, Power consumption verification

Case Study: overview of cellular phone design with emphasics on area optimization, speed improvement & power optimization.

References:

1. SudeepPasricha, NikilDutt, “On-Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann Publishers, 2008.
2. Rao R. Tummala, MadhavanSwaminathan, “Introduction to System on Package (SOP) – Miniaturization of the Entire System”, McGraw-Hill, 2008.
3. Hubert Kaselin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
4. B. Al Hashimi, “System on Chip – Next Generation Electronics”, The IET, 2006.
5. RochitRajsuman, “System-on-a-chip: Design and Test”, Advantest America R & D Center, 2000.
6. Michael J Flynn, Wayne Luk, “Computer System Design: System-on-chip”, Wiley Publications, 2011.

Course Outcomes (COs):

1. Compare SoB, SoC and SiP for electronic products in terms of size, cost, performance and reliability. (POs: 3, 4)
2. Analyze different approaches for solving architectural issues of SOC design (POs:1, 3, 4)
3. Discuss NISC and use of ADL. (POs: 1, 3, 4)
4. Recognize different simulation modes and modeling of reconfigurable systems. (POs: 1, 3, 4)
5. Appraise low power SOC design. (POs: 1, 3, 4)

PHYSICAL VLSI DESIGN

Course Code: MVEE12 **Credits: 4:0:0**

Prerequisites: CMOS VLSI Circuits **Contact Hours: 56**

Course Coordinator: Raghuram S

UNIT – I

Netlist Partition Algorithms: Introduction to electronic design automation, Algorithms and complexity, Graph theory terminology, Introduction to netlists and system partitioning

Partitioning Algorithms: Kernighan-Lin algorithm

UNIT – II

Chip Planning: Introduction, Optimization goals in floor planning, Floor plan representations

Floor Planning Algorithms: Floor plan sizing, Cluster growth, Simulated annealing, Pin assignment

Power and Ground Routing: Design of power-ground distribution network, Mesh routing, Integrated floor planning algorithms

UNIT – III

Global Placement and Routing: Introduction and objectives of placement, Global placement algorithms: min-cut placement, analytic placement, simulated annealing, Modern placement algorithms, Routing terminology and goals

Single-Net Routing: Rectilinear routing, Dijsktra's algorithm, A*, Full net routing and Rip-up and Re-route, Global routing in a connectivity graph, Modern global routing, Over the cell routing algorithms

UNIT – IV

Detailed and Specialized Routing: Building the horizontal and vertical constraint graphs, Left-edge algorithm, Dog-legging, Switchbox routing, Introduction to area routing, Non-Manhattan routing, Routing in clock networks, clock-tree synthesis

UNIT – V

Timing Closure: Introduction, Static timing analysis, Zero-slack algorithm, Timing driven placement, Timing driven routing, Physical synthesis, Performance driven design flow

References:

1. Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure", 1st Edition, Springer, 2011.
2. Sadiq M Sait, Habib Youssef, "VLSI Physical Design Automation", 1st Edition, World Scientific Publishing, 1995.
3. Navid A Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, Springer, 2005.

Course Outcomes (COs):

1. Employ basic partitioning algorithms to netlists. (POs: 3, 4)
2. Compute the area using different floor planning algorithms. (POs: 3, 4)
3. Predict the cost on the resultant wiring due to different place and route algorithms. (POs: 3, 4)
4. Apply routing algorithms to interconnect and clock networks. (POs: 3, 4)
5. Choose appropriate interconnections in the presence of timing constraints. (POs: 3, 4)

ADVANCED COMPUTER ARCHITECTURE

Course Code: MVEE13 **Credits: 4:0:0**

Prerequisites: Computer Organization **Contact Hours: 56**

Course Coordinator: Raghuram S

UNIT – I

Introduction to Processor: Introduction, Logic design conventions, Building a datapath, A simple implementation scheme

Instruction Sets: Computer hardware, Representing instructions in the computer, Instructions for making decisions, Sample instruction sets

UNIT – II

Program Flow Mechanisms: Control flow vs data flow, Comparisons of flow mechanisms, Performance metrics and measures, Data flow architecture, Demand driven mechanisms

Principles of Scalable Performance: Parallel processing applications, Speedup performance laws, Scalability analysis and approaches

UNIT – III

Speedup Performance Laws: Amdhal's law, Gustafson's law, Memory bounded speedup model

Advanced Processors: Advanced processor technology, Instruction-set architectures, CISC scalar processors, RISC scalar processors, Superscalar processors, VLIW architectures

UNIT – IV

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline, Design mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch handling techniques, Branch prediction, Arithmetic pipeline design

Memory Hierarchy Design: Cache basics and cache performance, Reducing miss rate and miss penalty, Multilevel cache hierarchies, Main memory organization, Design of memory hierarchies

UNIT – V

Multiprocessor Architectures: Symmetric shared memory architectures, Distributed shared memory architectures, Models of memory consistency

Graphics and Computing GPUs: Introduction, GPU system architecture, Programming GPUs, Multithreaded multiprocessor architecture, Parallel memory system, Floating point arithmetic, NVIDIA GeForce 8800 B-46, Mapping applications to GPUs

References:

1. Kai Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability", 1st Edition, Tata McGraw Hill, 2003.
2. David A Patterson, John L Hennessey, "Computer Organization and Design: The Hardware Software Interface", The Morgan Kaufmann [RISC-V Edition] 2017.
3. Kai Hwang, Zu, "Scalable Parallel Computers Architecture", Tata McGraw Hill, 2003.
4. M.J. Flynn, "Computer Architecture, Pipelined and Parallel Processor Design", Narosa Publishing, 2002.
5. D. A. Patterson, J. L. Hennessy, "Computer Architecture: A Quantitative Approach", Morgan Kauffmann, 2012.

Course Outcomes (COs):

1. Illustrate contemporary computer architecture issues and techniques. (POs: 1, 3, 4)
2. Discuss the role of parallelism in current and future architectures. (POs: 1, 3, 4)
3. Analyze the behavior of a processor pipeline executing sequences of instructions. (POs: 1, 3, 4)
4. Apply principle of cache and virtual memory for high performance computer architecture. (POs: 1, 3, 4)
5. Compare different multi-processor and GPU architectures for computing. (PO: 1, 3, 4)

VLSI SIGNAL PROCESSING

Course Code: MVEE14 **Credits: 4:0:0**

Prerequisites: Digital Signal Processing **Contact Hours: 56**

Course Coordinator: S. L. Gangadharaiah

UNIT – I

Introduction to DSP Systems: Typical DSP algorithms, DSP application demands and scaled CMOS technologies, Representations of DSP algorithms

Iteration Bounds: Data flow graph representations, Loop bound and iteration bound, Algorithms for computing iteration bound, Iteration bound of multirate data flow graphs

UNIT – II

Pipelining and Parallel Processing: Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power

Retiming: Definition and properties, Solving systems of inequalities, Retiming techniques

UNIT – III

Unfolding: An algorithm for unfolding, Properties of unfolding, Critical path, Unfolding and Retiming, Applications of unfolding

Folding: Folding transformation, Register minimization techniques, Register minimization in folded architectures

Fast Convolution: Cook-Toom algorithm, Winograd algorithm, Iterated convolution, cyclic convolution, Design of fast convolution algorithm by inspection

UNIT – IV

Algorithmic Strength Reduction Techniques: 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, Parallel rank-order filters, Look ahead pipelining in first-order IIR filters, Look ahead pipelining with power of 2 decomposition, Clustered look-ahead pipelining, Parallel processing for IIR filters, Combined pipelining and parallel processing for IIR Filter, Low power IIR filter Design using pipelining and parallel processing

UNIT – V

Bit-level Arithmetic Architectures: Parallel multipliers with sign extension, Parallel carry-ripple array multiplier, Parallel carry-savearray multiplier, Baugh –Wooley Multiplier, Parallel multipliers with modified booth recoding, Design of Lyon's bit-serial multipliers using Horner's rule, Bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed arithmetic

References:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems: Design and Implementation", Wiley, Interscience, 2007.
2. U. Meyer Baese, "Digital Signal Processing with Field Programmable Gate Arrays", 2nd Edition, Springer, 2004.
3. Roger Woods, John McAllister, Gaye Lightbody, Ying Yi, "FPGA based Implementationof Signal Processing Systems", John Wiley, 2008.
4. S. Y. Kung, H. J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
5. Jose E. France, YannisTsividis, "Design of Analog –Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
6. Lars Wanhammar, "DSP Integrated Circuits", 1st Edition, Academic Press Series in Engineering, 1999.

Course Outcomes (COs):

1. Enumerate use of various DSP algorithms and their representation using block diagrams, signal flow and dataflow graphs. (POs: 1, 3, 4)
2. Apply the concept of pipelining, retiming and parallel processing in design of high-speed low power applications. (POs: 1, 3, 4)
3. Employ unfolding, folding and fast convolution in the design of VLSI architecture (POs: 1, 3, 4)
4. Illustrate algorithmic strength reduction techniques to VLSI implementation of filters. (POs: 1, 3, 4)
5. Compare bit level arithmetic architectures for VLSI implementation of various DSP applications. (POs: 1, 3, 4)

MEMORY TECHNOLOGIES

Course Code: MVEE15 **Credits: 4:0:0**

Prerequisites: CMOS VLSI Circuits **Contact Hours: 56**

Course Coordinator: V. Anandi

UNIT – I

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM cell structures, MOS SRAM architecture, MOS SRAM cell and peripheral circuit, Bipolar SRAM, Advanced SRAM architectures, Application specific SRAMs

UNIT – II

DRAM: MOS DRAM Cell, BiCMOS DRAM, Error failures in DRAM, Advanced DRAM design and architecture, Application Specific DRAMs, SRAM and DRAM memory controllers

UNIT – III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar and CMOS PROM, EEPROMs, Floating gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash memories

UNIT – IV

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog memories, Magneto Resistive Random Access Memories (MRAMs), Experimental memory devices

UNIT – V

Memory Hybrids: Memory Hybrids – 2D & 3D, Memory stacks, Memory testing and reliability issues, Memory cards, High density memory packaging

References:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Publications, 2002.
2. Kiyoo Itoh, “VLSI Memory Chip Design”, 1st Edition, Springer Series in Advanced Microelectronics, 2001.

3. Ashok K Sharma, “Semiconductor Memories: Technology, Testing and Reliability”, PHI, 1997.

Course Outcomes (COs):

1. Recall random access memory classification and understand their operation. (POs: 1, 4)
2. Analyse the operation of advanced architectures of dynamic RAMs. (POs: 1, 4)
3. Differentiate between behavior of various ROMs and flash memories. (POs: 1, 4)
4. Illustrate understanding of contemporary and advanced memory technologies. (POs: 1, 4)
5. Apply concept of testing on memories and understand different memory packaging technologies. (POs: 1, 4)

COMMUNICATION BUSSES AND INTERFACES

Course Code: MVEE16 **Credits: 4:0:0**

Prerequisites: Analog Communication **Contact Hours: 56**

Course Coordinator: Mamtha Mohan

UNIT– I

Serial Busses: Physical interface, Data and control signals, features

UNIT – II

Serial Busses: Limitations and applications of RS232, RS485, I2C, SPI

UNIT– III

CAN: Architecture, Data transmission, Layers, Frame formats, applications

UNIT– IV

PCI: Revisions, Configuration space, Hardware protocols, applications

UNIT – V

UCB: Transfer types, enumeration, Descriptor types and contents, Device driver, Data streaming serial communication protocol – Serial Front Panel Data Port (SFPDP) using fiber optic and copper cables

References:

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", 2nd Edition, Lakeview Research, 2007.
2. Jan Axelson, "USB Complete", 5th Edition, Penram Publications, 2007.
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press, 2012.
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", 2nd Edition, Copperhill Media Corporation, 2005.

Course Outcomes (COs):

1. Recall various communications protocols and interface busses. (POs: 1, 4)
2. Illustrate understanding of contemporary serial busses and limitations. (POs: 1, 4)
3. Discuss CAN architecture and different frame formats. (POs:1, 3, 4)
4. Compare various hardware protocols and their applications. (POs: 1, 4)
5. Apply data transfer concepts and serial communication protocols on serial busses. (POs: 1, 4)